IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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3-2-01

Applicant(s):	Eliyahou Harari et. al.		
Title:	Flash EEprom System		
Serial No.:	09/188,417	Filing Date:	November 9, 1998
Examiner:	Phan, T.	Group Art Unit:	2818
Docket No.:	M-10187-30C US		

San Francisco, California
February 12, 2001

COMMISSIONER FOR PATENTS
Washington, D. C. 20231

AMENDMENT

Dear Sir:

In response to the Office Action mailed on October 11, 2000, and for which a one month extension is hereby requested, please kindly amend the above-identified patent application as follows:

IN THE SPECIFICATION

Replace the paragraph beginning on page 25, line 32 and ending on page 26, line 11 with the following:

--In the present invention, a system of Flash EEprom is used to provide non-volatile memory in place of traditional system memories such as disk storage. However, Flash EEprom memory is subject to wearing out by excessive program/erase cycles. Even with the improved Flash EEprom memory device as disclosed in co-pending U.S. patent applications, Serial No. 204,175, now patent no. 5,095,344, and one entitled "Multi-state EEprom Read and Write Circuits and Techniques," by Sanjay Mehrotra and Dr. Eliyahou Harari, Serial No. 07,337,579, filed April 13, 1989, now abandoned, the endurance limit is approximately 10^6 program/erase cycles. In a ten-year projected life time of the device, this translates to a limit of one program/erase cycle per 5 minutes. This may be marginal in normal computer usage.--

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